

**REMARKS**

Claims 6 through 10, 18, 19, 22, 23, 25 and 26 are currently pending in the application.

This is in response to the Office Action of March 7, 2002.

Claims 6 through 10, 18, 19, 22, 23, 25 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takashima et al. (U.S. Patent No. 5,838,038) in view of Eimori (U.S. Patent No. 5,610,418), Nakamura et al. (U.S. Patent No. 5,654,577) and Takahashi et al. (5,287,000).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants proffer the following remarks in support of the claimed invention which clearly distinguishes over the cited prior art.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Applicants submit that any proposed combination of the Takashima reference in view of the Eimori, Nakamura and Takahashi references does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of independent claims 6, 18 and 22, as well as dependent claims 7-10, 19, 23, 25 and 26, because, at the very least, the cited prior art does not teach or suggest all the claim limitations in sufficient detail that would enable a combination of the references to result in any operable combination. The Examiner's proposed combination of "a DRAM of cell size of  $2F \times 3F = 6F^2$ " of Takashima ('038) (col. 25, lines 17-18) with a design rule of adequate reduction, such as a 0.25 micron design rule from Eimori is improper. Specifically, while Takashima discloses that "a DRAM of cell size of  $2F \times 3F = 6F^2$  in which random access can be made and noise is small and which has trench capacitor type memory cells can be realized" (col. 25, lines 17-20), there is no disclosure of any

specific design rule for allowing any specific memory cell densities. Therefore, the Examiner has derived a specific design rule, namely 0.25 microns, as a design rule that would result in densities in accordance with those of the claimed invention. However, Eimori nor Takashima, either individually or in any proper combination, disclose how to make a  $6F^2$  memory cell using the design rule of 0.25 microns since the problems and solutions associated with shrinking Takashima's  $6F^2$  memory cell are not disclosed.

As disclosed in Applicants' specification, shrinkage of the memory cell, whether  $8F^2$  or  $6F^2$ , to reach a 0.6 micron memory cell pitch involves a number of significant problems. (Applicants' specification p. 2, line 19). As one example, as the minimum pitch falls below 1.0 micron, conventional "LOCAl Oxidation of exposed Silicon" (LOCOS) techniques fail due to excessive encroachment of the oxide beneath the masking stack. (Applicants' specification p. 7, lines 13-16). Furthermore, the memory cell storage node capacitance tends to decrease with the decrease in cell size, yet a minimum storage capacity for stored charge is required to maintain reliable operation. (Applicants' specification p. 8, lines 5-7). As yet another example of scaling issues, adequate spacing is required between adjacent devices, such as between a bit line contact and construction of a capacitor. (Applicants' specification p. 20, lines 3-6). Furthermore, field oxide regions, such as field oxide that is used to provide electrical isolation between certain adjacent banks of memory cells within an array, need to be eliminated to reduce size. (Applicants' specification p. 26, lines 7-11).

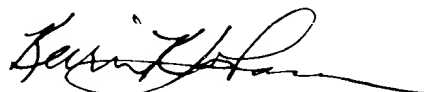
Additionally, bit line circuitry and bit line spacing affect the feasibility of shrinking an individual memory cell design within an array to a  $6F^2$  size. (Applicants' specification p. 27, line 23 to p. 28, line 1). Furthermore, the space consumed by the digit lines D and D\* and their associated circuitry become one of the limiting factors for conversion to a  $6F^2$  size. (Applicants' specification p. 28, lines 15-17). All of the aforementioned design considerations would need to be addressed in order for the memory cell as disclosed by Takashima to be shrunk to a 0.6um memory cell resulting in the densities as claimed by Applicants in independent claim 6. As a further example, the memory cell of Takashima as illustrated in Figure 28, includes LOCOS isolation, illustrated as oxide 133 under the word lines and between adjacent memory cells, with spacing also illustrated between bit line contacts and storage nodes. A simple reduction in the

photolithographic feature size would result in the problems that are identified and addressed only by Applicants' invention as claimed.

Therefore, Applicants' respectfully request that the rejection of independent claims 6, 18 and 22 and claims 7-10, 19, 23, 25 and 26 depending therefrom be withdrawn. Applicants submit that claims 6 through 10, 18, 19, 22, 23, 25 and 26 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 6 through 10, 18, 19, 22, 23, 25 and 26 and the case passed for issue.

Respectfully submitted,



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